REMARKS/ARGUMENT

This preliminary amendment is being submitted to make the formal amendments that were made in the parent application, and further to emphasize patentable subject matter in new claims 29-44. These claims are supported by Fig. 1A and the corresponding text.

As recited in claim 29, each active trench has a polysilicon plug of one conductivity type; while each intermediate trench has a polysilicon plug of the opposite conductivity type; each of the intermediate trenches further having a shallow diffusion of said opposite conductivity type extending from its walls; and the intermediate trenches and the source regions being connected in common to the source contact.

According to claims 30, 33 and 35, the source regions disposed respectively between each pair of active and intermediate trenches are of the one conductivity type.

The prior art of record is not seen to disclose at least this combination of features.

For at least these reasons, in addition to other patentable subject matter therein, allowance of claims 29-44 is requested.

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Respectfully submitted,

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APPENDIX B
VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph at page 2, line 16 to line 20:

Because of these diverse requirements, different manufacturing processes are used for a "megarad" product, designed for use in a high total radiation dose environment, and an SEE product which is optimized for single particle effects.

Paragraph at page 3, line 1 to line 17:

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the present invention a MOSgated device (a power MOSFET, IGBT, GTO or other device employing a [an] MOS gate) which has optimal oxide thicknesses for both total radiation dose resistance and SEE resistance is provided, using a trench design device. Thus, a known vertical conduction trench device has an invertible channel region on the sides of each trench, while the drift region lies along and under the bottoms of the trenches. Consequently, the gate oxide thickness at the walls of each [the] trench can be relatively thin, and less than about 900 Å (preferably about 500 Å) for optimal total dose resistance, while the bottoms of the trenches [trench] have a relatively thick oxide liner, for example, greater[,] than about 1300 Å (and preferably about 3000 Å) for optimal resistance to breakdown by single event effects.

Paragraph at page 5, line 6 to line 17:

Thereafter, the wells 20 to 23 are filled with conductive N+ polysilicon layers 50 to 53 which act as the conductive gates for the device and which are laterally interconnected (not shown) and have an appropriate common gate connection terminal G [60]. The tops of polysilicon layers 50 to 53 are covered by patterned oxide insulation layers 60 to 63 respectively.

The upper surface of the device then receives an aluminum source electrode 70 which is connected to the exposed regions of source regions 14 to 17, and to the P regions 13 between the sources. A drain electrode 71 is formed on the bottom of chip 10.

Insert Paragraph at page 6 between lines 8 and 9:

Trenches containing MOS gated structure 20, 21 may be polygonal in topology and may be symmetrically spaced and disposed over the surface of the chip 10. Source regions 14, 15 surround trenches 20, 21, respectively, containing MOS gated structure. Intermediate trenches 80-82 may consist of a trench of lattice shape in topology extending in the space defined between spaced polygonal trenches 20, 21.

Paragraph at page 9, line 25 to page 10, line 3:

The trenches may provide a plurality of floating rings, or at least one floating ring. The precise number of trenches used and their spacing can be optimized for each voltage rating. Thus, more rings with wider spacing are used for higher voltage devices and fewer rings at closer spacing are used for lower voltage ratings. For example, for a high voltage termination, the rings may be spaced by 3 to 5 microns. For a lower voltage termination, the rings could be spaced from 1.5 to about 2 microns. The wider spaced rings will break down at a lower voltage than closer spaced rings.

CLAIMS (with indication of amended or new):

(NEW) 29. A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches; and

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches;

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches.

(NEW) 30. The device of claim 29, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 31. The device of claim 30, wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

(NEW) 32. The device of claim 29, wherein all of said active trenches are parallel elongated trenches.

(NEW) 33. The device of claim 32, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 34. The device of claim 29, wherein:

at least a plurality of said active trenches containing MOS gated structures are polygonal in topology and are symmetrically spaced and disposed over the surface of said silicon wafer;

said source regions surrounding respective ones of said active trenches containing a MOS gated structure;

said intermediate trenches surrounding said at least a plurality of said active trenches consisting of a trench of lattice shape in topology which extends in the space defined between spaced active trenches having said polygonal to pology.

(NEW) 35. The device of claim 34, in which said source regions between said active and intermediate trenches are of said one conductivity type.

(NEW) 36. The device of claim 29, wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE.

(NEW) 37. The device of claim 36, in which said gate dielectric and said bottom dielectric are silicon dioxide.

(NEW) 38. The device of claim 37, wherein said gate dielectric has a thickness which is less than 900 Å.

(NEW) 39. The device of claim 38, wherein the thickness of said bottom dielectric is greater than about 1300 Å.

(NEW) 40. The device of claim 37, wherein the thickness of said bottom dielectric is greater than about 1300 Å.

(NEW) 41. The device of claim 36, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches

and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(NEW) 42. The device of claim 10, wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(NEW) 43. The device of claim 42, wherein said concentric rings have a predetermined spacing from one another.

(NEW) 44. The device of claim 43, wherein the spacing between said rings is selected such that breakdown caused by high reverse voltage occurs between said rings before breakdown occurs in said active area.